N-channel enhancement mode Logic level TrenchMOS™ transistor

IRLZ34N

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in switched mode power supplies and general purpose switching applications.

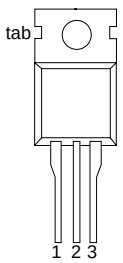
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	30	A
P_{tot}	Total power dissipation	68	W
T_j	Junction temperature	175	˚C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	35	mΩ

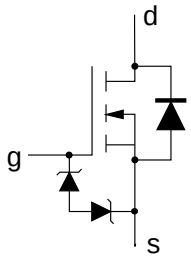
PINNING - TO220AB

PIN	DESCRIPTION
1	gate
2	drain
3	source
tab	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 175˚C	-	55	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 175˚C; R_{GS} = 20 kΩ	-	55	V
V_{GS}	Gate-source voltage		-	± 13	V
I_D	Continuous drain current	T_{mb} = 25 ˚C	-	30	A
		T_{mb} = 100 ˚C	-	21	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	110	A
P_D	Total power dissipation	T_{mb} = 25 ˚C	-	68	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	2.2	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient		60	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

ELECTRICAL CHARACTERISTICS

T_j= 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	55	-	-	V
		T_j = -55˚C	50	-	-	V
$V_{(BR)GSS}$	Gate-source breakdown voltage	I_G = ±1 mA;	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	1.0	1.5	2.0	V
		T_j = 175˚C	0.5	-	-	V
		T_j = -55˚C	-	-	2.3	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 5 V; I_D = 17 A	-	28	46	mΩ
		V_{GS} = 10 V; I_D = 17 A	-	26	35	mΩ
		T_j = 175˚C	-	-	74	mΩ
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	12	40	-	S
I_{GSS}	Gate source leakage current	V_{GS} = ±5 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 55 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
$Q_{g(tot)}$	Total gate charge	I_D = 30 A; V_{DD} = 44 V; V_{GS} = 5 V	-	22.5	-	nC
Q_{gs}	Gate-source charge		-	6	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	11	-	nC
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	14	21	ns
t_r	Turn-on rise time	V_{GS} = 5 V; R_G = 10 Ω	-	77	110	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	55	80	ns
t_f	Turn-off fall time		-	48	65	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	1050	1400	pF
C_{oss}	Output capacitance		-	205	245	pF
C_{rss}	Feedback capacitance		-	113	150	pF

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_S	Continuous source current (body diode)		-	-	30	A
I_{SM}	Pulsed source current (body diode)		-	-	110	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 34 A; V_{GS} = 0 V	-	1.0	-	V
t_{rr}	Reverse recovery time	I_F = 34 A; -dI_F/dt = 100 A/µs;	-	40	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.16	-	µC

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AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 20 A; $V_{DD} \leq$ 25 V; V_{GS} = 5 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	45	mJ

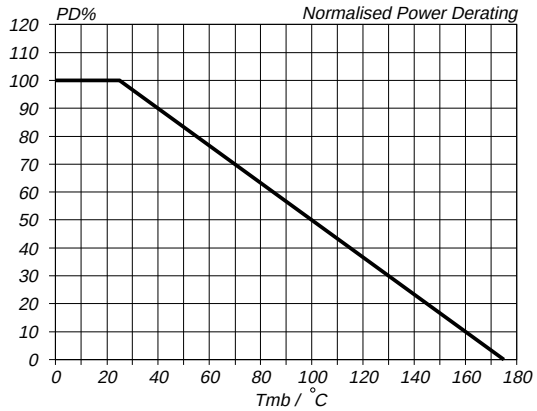

Fig.1. Normalised power dissipation. PD% = 100·P_D/$P_{D\ 25\ ˚C}$ = f(T_{mb})

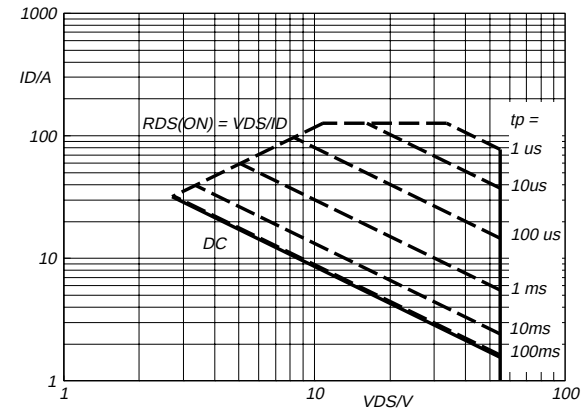

Fig.3. Safe operating area. T_{mb} = 25 ˚C I_D & I_{DM} = f(V_{DS}); I_{DM} single pulse; parameter t_p

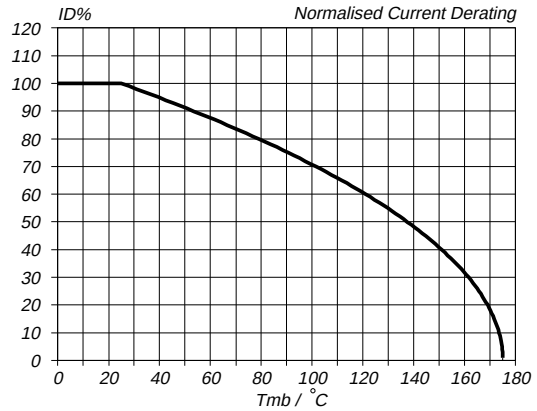

Fig.2. Normalised continuous drain current. ID% = 100·I_D/$I_{D\ 25\ ˚C}$ = f(T_{mb}); conditions: $V_{GS} \geq$ 5 V

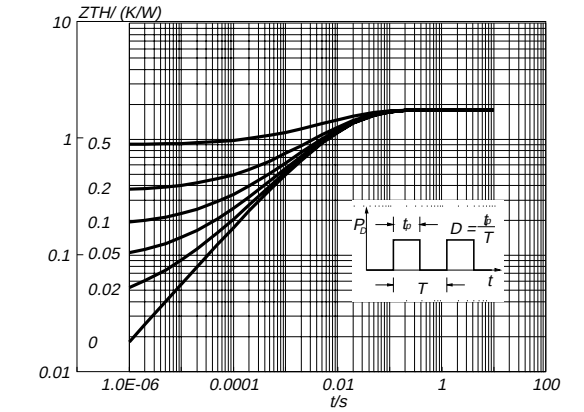

Fig.4. Transient thermal impedance. $Z_{th\ j\text{-}mb}$ = f(t); parameter D = t_p/T

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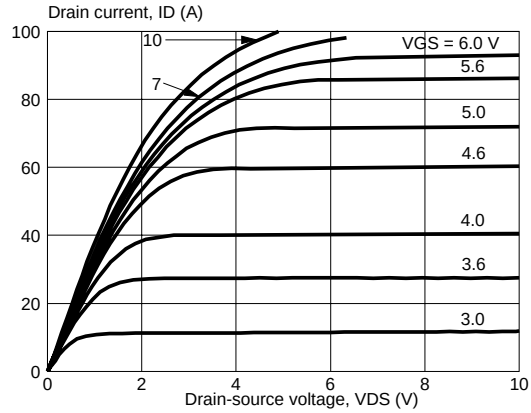

Fig.5. Typical output characteristics, T_j = 25 ˚C. $I_D = f(V_{DS})$; parameter V_{GS}

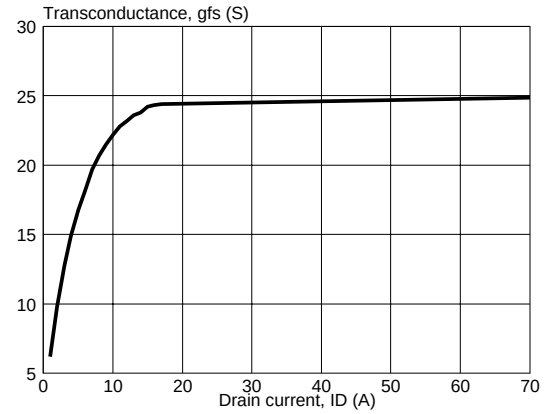

Fig.8. Typical transconductance, T_j = 25 ˚C. $g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

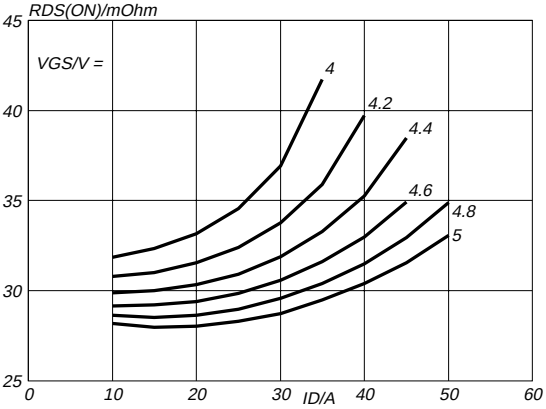

Fig.6. Typical on-state resistance, T_j = 25 ˚C. $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

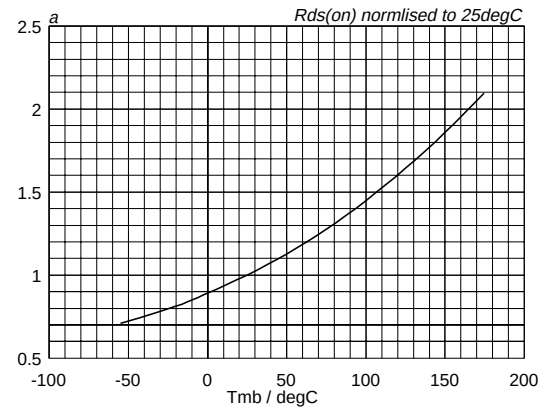

Fig.9. Normalised drain-source on-state resistance. $a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 17 A; V_{GS} = 5 V

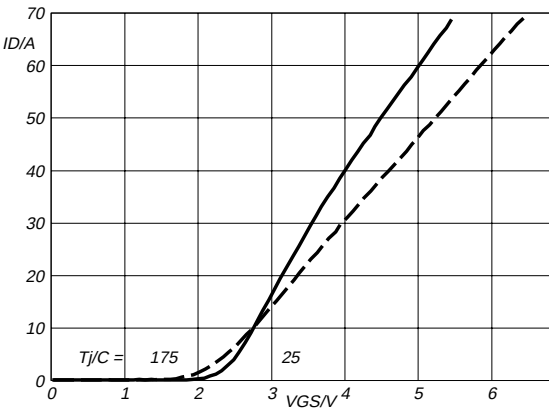

Fig.7. Typical transfer characteristics. $I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

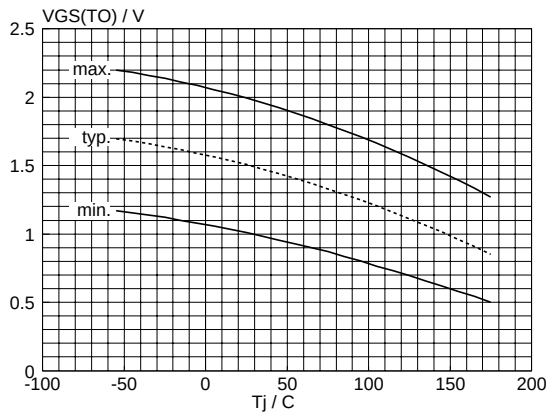

Fig.10. Gate threshold voltage. $V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

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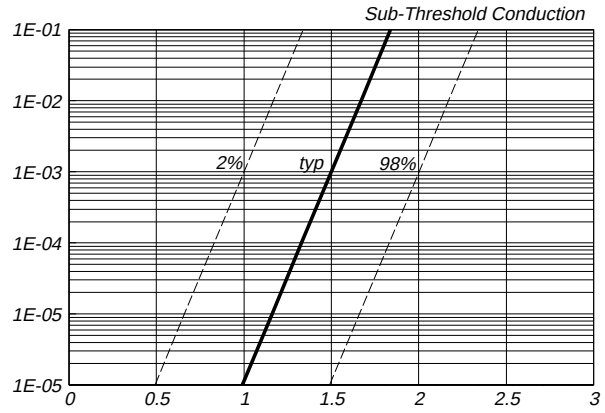


Fig.11. Sub-threshold drain current.
I_D = f(V_{GS}); conditions: T_j = 25 ˚C; V_{DS} = V_{GS}

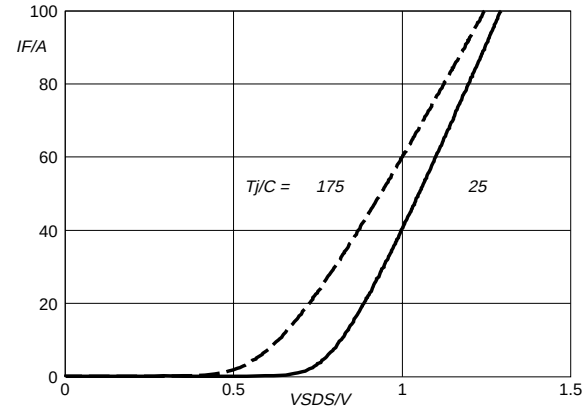


Fig.14. Typical reverse diode current.
I_F = f(V_{SDS}); conditions: V_{GS} = 0 V; parameter T_j

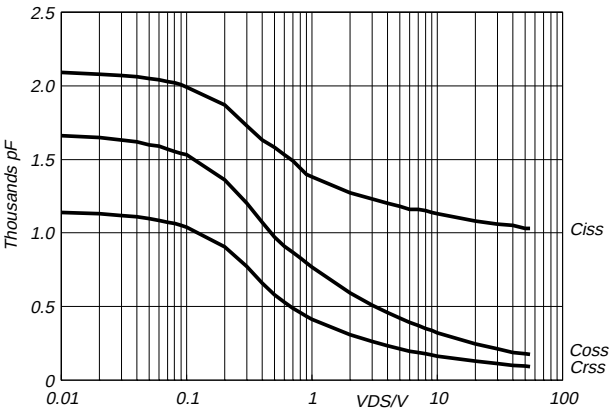


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
C = f(V_{DS}); conditions: V_{GS} = 0 V; f = 1 MHz

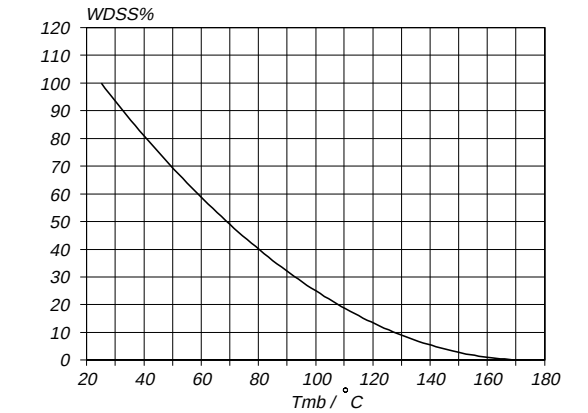


Fig.15. Normalised avalanche energy rating.
W_{DSS}% = f(T_{mb}); conditions: I_D = 20 A

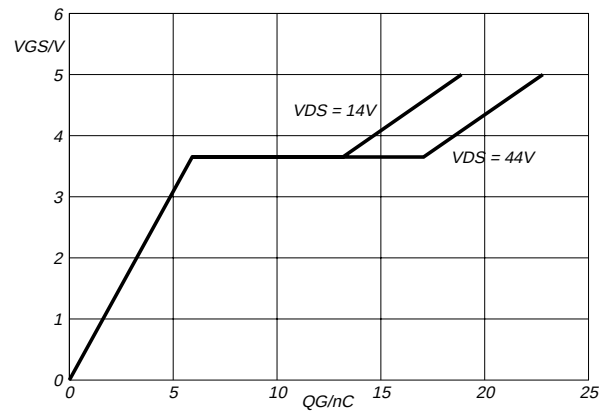


Fig.13. Typical turn-on gate-charge characteristics.
V_{GS} = f(Q_G); conditions: I_D = 30 A; parameter V_{DS}

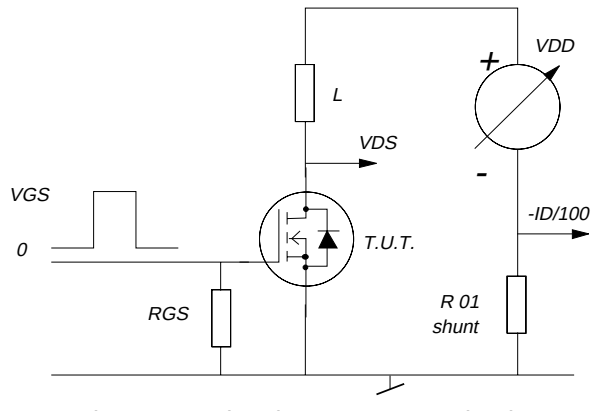
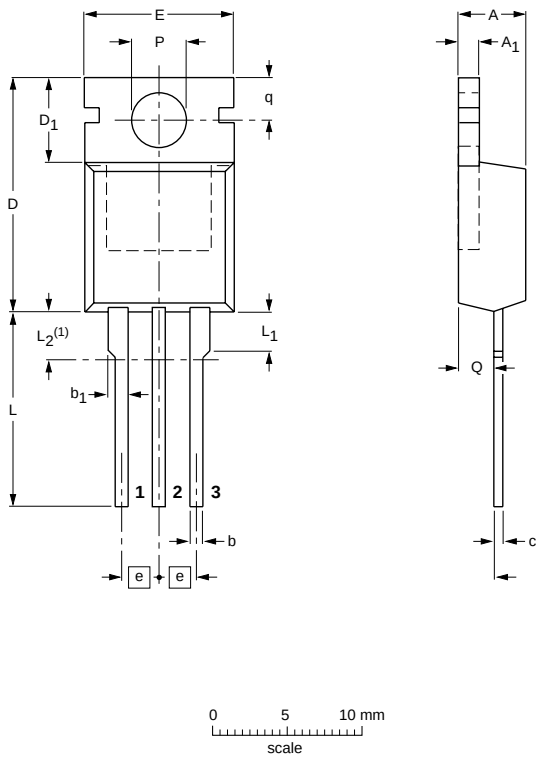


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

MECHANICAL DATA

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220 **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	$L_2^{(1)}$ max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220				97-06-11

Fig.17. SOT78 (TO220AB); pin 2 connected to mounting base (Net mass:2g)

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to mounting instructions for SOT78 (TO220AB) package.
3. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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